

# Existence of Optimum Cold FET Intrinsic Reference Plane for Active FET Small Signal Modeling

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**Abstract**—Cold FET methods have been widely used for active FET modeling assuming the bias independence of parasitic elements. However, the assumption has been merely justified by the resulting modeling accuracy. This paper investigates the consistency of cold FET conditions with active FET through the exact and the error minimizing solutions of cold FET intrinsic reference plane constrained by the feedback condition of active FET model. Additionally, drain bias dependence of parasitic resistances will be presented.

**Index Terms**—Active small signal modeling, cold FET methods, intrinsic reference plane.

## I. INTRODUCTION

FOR THE last ten years, cold FET methods have been successfully used for direct determination of FET small signal model parameters [1], [2] under the assumption of bias independence of parasitic elements, which strictly means the invariance of intrinsic reference plane from cold FET to hot FET. However, there still remain unresolved problems for cold parasitic resistances, which resultantly define the intrinsic reference plane of an active FET. Since usual cold FET measurements yield only 3 independent conditions for four resistive elements [1], an additional condition is essential. Several methods have been proposed for exact determination [1], [3]–[5], but the results are not always the same because the intrinsic models are different from each other. In addition to the problem of exact determination, the basic question that using cold FET reference plane is valid for modeling the FET in the saturation region has not been conclusively answered except through *a posteriori* validation based on the resulting accuracy of small signal modeling.

If three cold FET conditions are used and active intrinsic ECPs can be uniquely determined after parasitic de-embedding, the small signal modeling has only one degree of freedom. Especially for 7-element intrinsic model in Fig. 1, it constitutes an exact problem because the real part of the intrinsic feedback admittance in the saturation region is to be zero as indicated by [6]. Then, it is doubtful that cold FET conditions can provide an intrinsic reference plane meeting the constraint. If it is not true, it wonders if there exists the most closely mating cold reference plane with the active model. This letter presents the exact and the error minimizing solutions of the cold FET resistive parameters

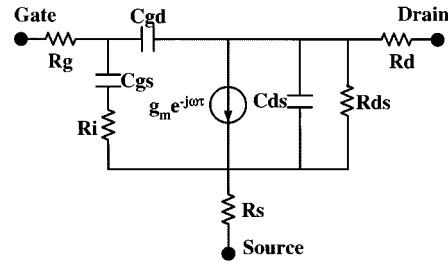


Fig. 1. FET small signal model in the saturation region.

constrained by the intrinsic feedback condition of the 7-element small signal model. These solutions will clearly show whether the cold FET conditions are consistent with the active intrinsic model. In the remainder of this letter, reactive parasitics are adequately de-embedded using the methods in [7].

## II. DETERMINATION OF COLD FET INTRINSIC REFERENCE PLANE

It is well known that cold FET measurements yield following three deterministic conditions as used by [1] and originally derived by [3]

$$R_\alpha = R_c/3 + R_g + R_s \quad (1)$$

$$R_\beta = R_c/2 + R_s \quad (2)$$

$$R_\gamma = R_c + R_d + R_s \quad (3)$$

where  $R_c$  is a cold FET channel resistance. Though these conditions were initially derived at forward gate bias, equivalent conditions can be obtained under normal operating gate bias condition [7]. Cold parasitic resistances can be expressed as linear functions of  $R_c$ .

$$R_s = R_\beta - R_c/2 \quad (4)$$

$$R_g = R_\alpha - R_\beta + R_c/6 \quad (5)$$

$$R_d = R_\gamma - R_\beta - R_c/2. \quad (6)$$

If  $R_c$  is fixed, the parasitic resistances can be uniquely determined. Unfortunately, cold FET measurements do not yield a reliable additional independent condition, which means that there is no preferred intrinsic reference plane for  $R_c$  in the cold FET model. On the other hand, the intrinsic equivalent circuit of Fig. 1 imposes the definite constraint on the intrinsic reference plane, because the real part of the intrinsic feedback admittance is to be zero. If the assumption of bias independence of parasitic resistances is valid, active intrinsic admittances can be ex-

Manuscript received February 27, 2001; revised May 15, 2001. The review of this letter was arranged by Associate Editor Dr. Arvind Sharma.

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Publisher Item Identifier S 1531-1309(01)06579-5.

pressed with extrinsic  $Z$  parameters and cold FET resistances as follows.

$$\begin{aligned} \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} &= \begin{bmatrix} Z_{11} - R_\alpha + R_c/3 & Z_{12} - R_\beta + R_c/2 \\ Z_{21} - R_\beta + R_c/2 & Z_{22} - R_\gamma + R_c \end{bmatrix}^{-1} \\ &= \begin{bmatrix} \zeta_{11} + R_c/3 & \zeta_{12} + R_c/2 \\ \zeta_{21} + R_c/2 & \zeta_{22} + R_c \end{bmatrix}^{-1}. \end{aligned} \quad (7)$$

In (7),  $Z_{ij}$ s subtracted by  $R_\alpha$  and  $R_\beta$  or  $R_\gamma$  are represented by  $\zeta_{ij}$ s. Then,  $y_{12}$  is given by

$$y_{12} = -j\omega C_{gd} = -\frac{\zeta_{12} + R_c/2}{\Delta_z} = -\frac{(\zeta_{12} + R_c/2)\Delta_z^*}{|\Delta_z|^2} \quad (8)$$

where

$$\Delta_z = \begin{vmatrix} \zeta_{11} + R_c/3 & \zeta_{12} + R_c/2 \\ \zeta_{21} + R_c/2 & \zeta_{22} + R_c \end{vmatrix}$$

and  $*$  means the conjugate.

Since the real part of  $y_{12}$  is zero, following equation should be satisfied.

$$\text{Re}((\zeta_{12} + R_c/2)\Delta_z^*) = 0. \quad (9)$$

Finally, (9) can be arranged as a third-order equation of  $R_c$

$$a_3 R_c^3 + a_2 R_c^2 + a_1 R_c + a_0 = 0 \quad (10)$$

where the respective coefficients are

$$\begin{aligned} a_0 &= -\text{Im}(\zeta_{12})^2 \text{Re}(\zeta_{21}) \\ &\quad + \text{Im}(\zeta_{12})[\text{Im}(\zeta_{22})\text{Re}(\zeta_{11}) + \text{Im}(\zeta_{11})\text{Re}(\zeta_{22})] \\ &\quad - \text{Re}(\zeta_{12})[\text{Im}(\zeta_{11})\text{Im}(\zeta_{22}) + \text{Re}(\zeta_{12})\text{Re}(\zeta_{21}) \\ &\quad \quad - \text{Re}(\zeta_{11})\text{Re}(\zeta_{22})] \end{aligned} \quad (11)$$

$$\begin{aligned} a_1 &= 1/6[6\text{Im}(\zeta_{11})\text{Im}(\zeta_{12}) - 3\text{Im}(\zeta_{12})^2 \\ &\quad - 3\text{Im}(\zeta_{11})\text{Im}(\zeta_{22}) \\ &\quad + 2\text{Im}(\zeta_{12})\text{Im}(\zeta_{22}) + 6\text{Re}(\zeta_{11})\text{Re}(\zeta_{12}) - 3\text{Re}(\zeta_{12})^2 \\ &\quad - 6\text{Re}(\zeta_{12})\text{Re}(\zeta_{21}) + 3\text{Re}(\zeta_{11})\text{Re}(\zeta_{22}) \\ &\quad + 2\text{Re}(\zeta_{12})\text{Re}(\zeta_{22})] \end{aligned} \quad (12)$$

$$a_2 = 1/12[6\text{Re}(\zeta_{11}) - 2\text{Re}(\zeta_{12}) - 3\text{Re}(\zeta_{21}) + 2\text{Re}(\zeta_{22})] \quad (13)$$

$$a_3 = 1/24. \quad (14)$$

Though (10) has three algebraic solutions, only one has reasonable magnitude.

Analytically solved  $R_c$  may show frequency dependence due to measurement noise, or more basically, inconsistency of the cold FET reference plane with the active FET. Then, it is necessary to investigate the existence of the most closely mating cold FET intrinsic reference plane with the active FET. For a given value of  $R_c$ , the cold parasitic resistances and accordingly the residual real part of de-embedded  $y_{12}$  of the active FET is definitely determined. Therefore, it is possible to find the optimum  $R_c$  minimizing the following residual feedback error

$$\frac{1}{N} \sqrt{\sum_{i=1}^N \text{Re}(y_{12})_i^2} \quad (15)$$

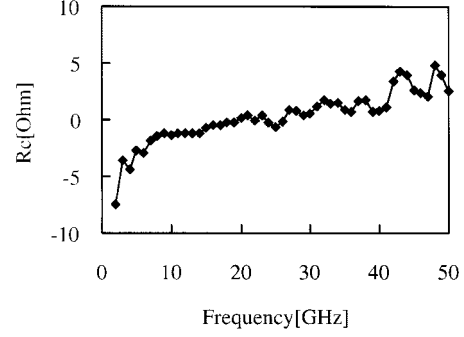


Fig. 2. Frequency dependence of the exact solution of the cold FET channel resistance  $R_c$ . Cold bias conditions at  $V_{gs} = 0.2$  V,  $V_{ds} = 0$  V, and active  $S$  parameters measured at  $V_{gs} = 0.2$  V and  $V_{ds} = 3.4$  V, are used.

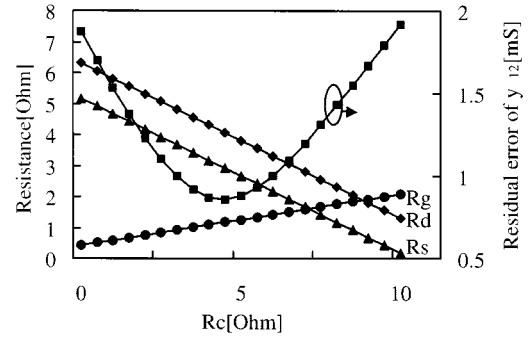


Fig. 3. Evolution of the residual error of the active intrinsic feedback admittance  $y_{12}$  as a function of  $R_c$ . Corresponding variations of the cold parasitic resistances determined by (4)–(6) are given in the primary Y-axis. Cold and active bias points are identical to those of Fig. 2.

where  $N$  is the number of measured frequencies. Since (15) is a single variable function of  $R_c$ , its minimum, if exists, can be easily found through error tracking. If (15) exhibits a minimum at a value of  $R_c$ , the cold parasitic resistances determined from (4)–(6) will provide an optimum intrinsic cold reference plane for a given active bias point.

### III. RESULTS

Fig. 2 shows the exact solution of  $R_c$  for  $0.3 \mu\text{m} \times 80 \mu\text{m}$  PHEMT device. Frequency dependence is not negligible, and therefore the simple average value will not be satisfactory. The cold FET conditions seem to be inconsistent with the active small signal model in the analytic sense. However, the residual error (15) of de-embedded  $y_{12}$  shows the unique minimum along the path of  $R_c$ , as shown in Fig. 3. Therefore, there exists a unique intrinsic cold reference plane preferred by the active small signal model at a given bias point. The value of error minimizing  $R_c$  is found around that of the exact solution in the highest measurement frequency range. The residual error measure is experimentally found to be robust for various MESFETs and HEMTs with different gate lengths and widths, except Si-MOSFETs. Though  $0.35 \mu\text{m} \times 80 \mu\text{m}$  NMOS was tested, the error minimum was not found.

The optimum  $R_c$  varies with the active bias point and, therefore, the cold parasitic resistances are also changed. Fig. 4 shows the drain bias dependence of the parasitic resistances by using error minimizing  $R_c$  at each bias point.  $R_s$  and  $R_d$  increase as

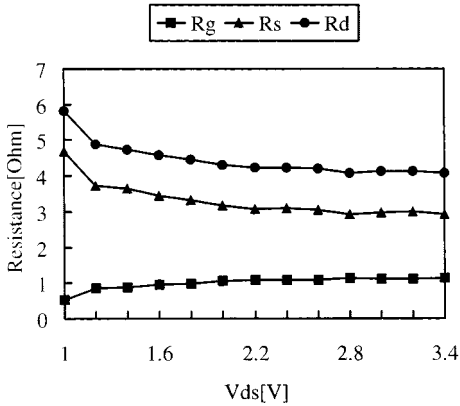


Fig. 4. Drain bias dependence of cold parasitic resistances determined by the residual error measure at  $V_{gs} = 0.2$  V. Cold FET conditions at  $V_{gs} = 0.2$  V,  $V_{ds} = 0$  V are used.

drain bias approaches the linear region. These increases do not mean the actual variation of  $R_s$  and  $R_d$  of the active FETs, but the extension of the cold FET intrinsic reference plane toward the channel region from each side of source and drain contacts. It is necessary to minimize the feedback error of the active intrinsic model. In the linear region, where the resistive feedback of intrinsic  $y_{12}$  cannot be ignored, the error minimizing  $R_c$  does not exist. To enhance the modeling accuracy and compensate the variance of the cold FET reference plane, a bias dependent resistance is needed in the feedback branch. Direct determined ECPs using the cold reference plane of Fig. 3 show  $S$  parameter modeling error below 5% at bias points given in Fig. 4.

#### IV. CONCLUSION

This letter has presented the exact and the error minimizing solutions of the cold parasitic resistances constrained by the seven-element active ECPs. The results show that the cold FET conditions may seem to be analytically inconsistent with the active small signal model. However, there exists optimum cold FET reference plane in the error minimizing sense at each bias point and its bias dependence is not so severe in the saturation region.

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